Integration of CMOS-electronics and particle detector diodes in high-resistivity silicon-on-insulator wafers

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(Detector R&D Collaboration RD19)

Abstract

A new approach to monolithic pixel detectors, based on SOI wafers with high resistivity substrate, is being pursued by the CERN RD19 collaboration. This paper reports on the used fabrication methods, and on the results of the electrical evaluation of the SOI - MOSFET devices and of the detector structures fabricated in the bulk. The leakage current of the high-resistivity PIN-diodes was kept in the order of 5 to 10 nA/cm^2. The SOI preparation processes considered (SIMOX and ZMR) produced working electronic circuits and appear to be compatible with the fabrication of detectors of suitable quality.

I. INTRODUCTION

The availability of "intelligent" pixel detectors, with a typical element size of the order of 100 μm, would be a precious resource for inner tracking and vertex detection in the next generation of extremely high luminosity colliders. In order to take advantage of the unambiguous pattern recognition capability of these detectors, and meet the speed and signal/noise requirements, a substantial amount of signal processing and control electronics must be located within the area of each pixel. This may be realized in either a hybrid (flip-chip) or a monolithic technology. The monolithic option offers potential benefits.

Monolithic co-integration of detectors and read-out electronics in high-resistivity silicon substrates has been reported before [1-5,9]. Although promising, these approaches showed serious disadvantages. In ref. [1-2], two-sided processing of the wafers is required. The approach in ref. [3-4] yields a geometrical fill-factor for the detectors below100%, unless serious limitations are accepted in the type of read-out electronics. Neither method allows the use of full CMOS circuitry.

Recently a different approach to monolithic devices has been pursued in the CERN RD-19 collaboration. Here, the detector diodes are fabricated in a high resistivity silicon substrate, while the CMOS electronic devices are located in an overlying SOI laver [6-7].

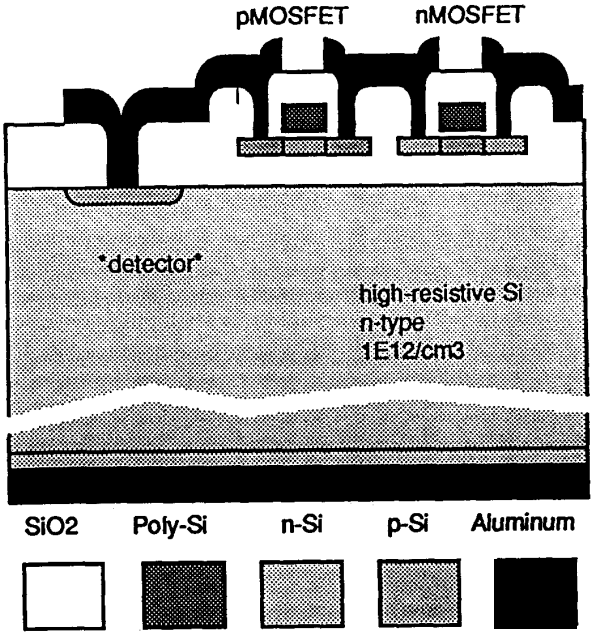

Fig.1 Schematic cross section of a processed SOI wafer with top layer electronics. (i.e. interconnects and complementary

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MOSFETs) that are connected to a PIN diode in the high-resistivity bulk material.

The development at IMEC explores the possibility to process CMOS circuits in either SIMOX ("separation by implantation of oxygen") or ZMR ("zone melt recrystallization") layers on top of high resistivity substrates (fig. 1). This combination promises the following benefits:
•well-established CMOS design method and good compatibility with earlier designs
•relative radiation hardness of SOI compared to bulk processes
•there is no need for hybridization of detectors with external electronics. The mass will be lower, the reliability higher, with less parasitic effects. Yet the geometrical fill factor can be 100%. Also very narrow pitch detectors will become feasible.
•Costs will decrease if wafers are processed in larger numbers.

The price to pay for the elegance of such an SOI approach is a slightly more complex processing. SOI fabrication techniques or process temperature steps may influence the quality of the high-resistivity material. Also, the presence of electronics close to the detector will cause electrical interference or cross-talk.

The emphasis is on studying the compatibility of the SOI wafer preparation processes considered with the properties required from a high resistivity substrate in order to obtain detectors of suitable quality. In particular, the SIMOX process, involving a very heavy oxygen implant and an extended (typically 6 hours) anneal at high temperature (around 1360 °C), is worrying because of the possible introduction of contaminants or structural defects. This may results in high leakage currents, signal charge trapping, unpractical depletion voltages in the detectors. ZMR requires a lower (but still high) temperature process; here however the non-uniform heating of the wafer is another possible source of crystal defects.

II. FEASIBILITY STUDY

In the first phase of the project, completed in 1991, a preliminary "feasibility" study has been performed. High resistivity wafers (4", 400 μm thick, FZ 5 kΩcm n-type <100>) were subjected to 3 SOI layer fabrication methods:
•SIMOX (separation by implantation of oxygen)
•laser ZMR (zone melt recrystallization by laser heating)
•Strip heater ZMR (zone melt recrystallization by halogen lamp heating)
Subsequently the top layer was stripped off, and the material quality was evaluated with a simple diode process for two main characteristics: diode leakage and possible dopant concentration increase.

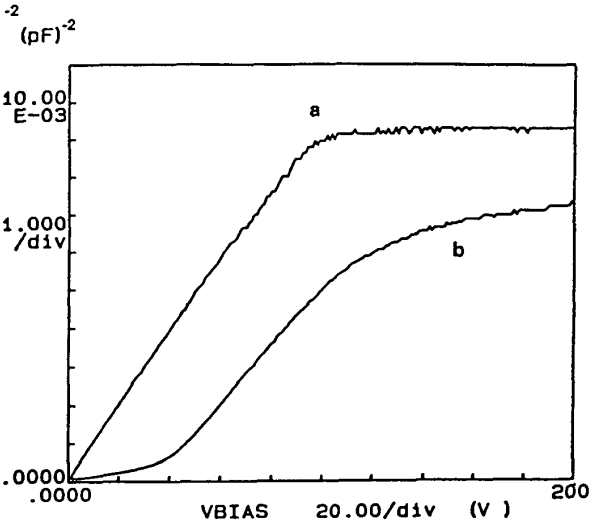

Fig.2 $1/C^2$ versus bias voltage for 0.38 cm^2 diodes on: a) laser ZMR substrate, b) SIMOX substrate. f = 1MHz.

Fig. 2a shows the $1/C^2$ versus V slope for a diode on a ZMR wafer. The constant slope indicates a uniform dopant concentration in the bulk ($N_D=8x10^{11}cm^{-3}$), and a total depletion voltage of about 100 V can be deduced from the saturation point. The corresponding curve for a SIMOX wafer (Fig. 2b) shows non-uniform doping and a still not totally depleted substrate at 200V bias. A doping profile extending almost to the back surface of the substrate is shown in fig.3. Two peaks in the net effective donor concentration are present, at about 50 μm distance from the front and back surfaces of the wafer. In the central region the dopant density is the same as for the ZMR samples, while the peaks are about an order of magnitude higher. Low temperature DLTS measurements performed on the samples are consistent with the hypothesis that these effective dopants are double oxygen donors, originating from the SIMOX implant and subsequent thermal treatments.

The effect of SOI fabrication processes on the carrier generation lifetime of the substrates are deduced from reverse-biased I-V measurements. The lowest currents were obtained from the ZMR wafers (fig. 4a). Approximately uniform carrier generation in the bulk dominates the current, as can be seen from the shape of the I-V curve, roughly following a square root dependence, and saturating at total depletion of the substrate. For this device , a carrier generation lifetime of about 0.25 ms can be calculated. On SIMOX wafers leakage currents were higher; an example is shown in Fig.4b, corresponding to a generation lifetime of 0.08 ms.

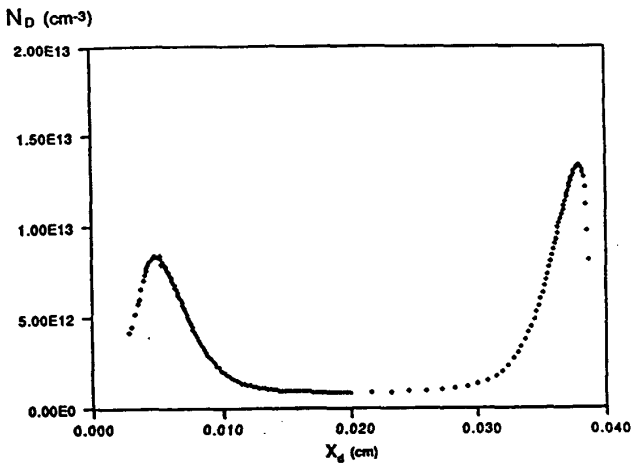

Fig.3 Profile of effective donor density versus depletion depth in the SIMOX substrate. This plot has been obtained from the combination of two 1 MHz C-V measurements: the first one covers the region up to 100 V bias, while the second extends to 400 V.

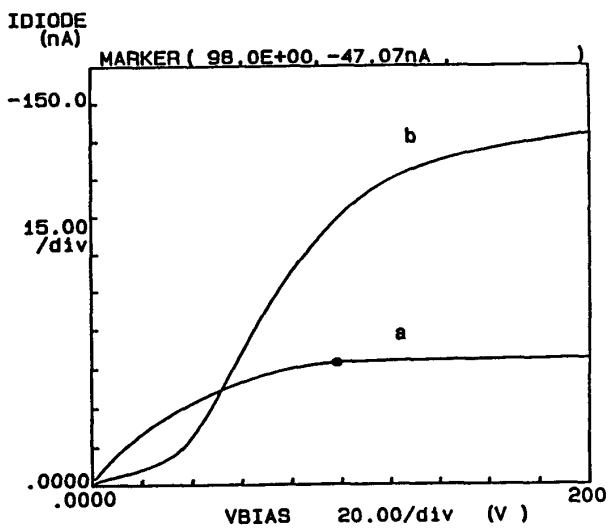

Fig.4 Reverse leakage current versus bias voltage for the same diodes as in Fig. 2

While these lifetimes are one to three orders of magnitude smaller than the best silicon detectors, they are still perfectly adequate for small volume devices: with a 80 μs lifetime, in a (100 μm)^2 pixel, 200 μm thick, the bulk generation would only contribute 20 pA at room temperature (23 °C). Furthermore, the main foreseen applications for such devices will be in heavy radiation environments, with high neutron and charged particle fluxes, where the lifetime is doomed to decrease to much lower levels during operation of the detector. In SIMOX wafers, the regions of increased dopant density do not appear to feature significantly higher thermal generation. They might have an effect on the charge collection efficiency by trapping - yet we see no evidence of slow trapping in the C-V measurements. Studies of this aspect, using ionizing particles or IR-light, are under way, as well as test of possible interactions of the SIMOX-related defects with displacement damage caused by e.g. neutron irradiation.

The conclusion of the study was that all three methods are suited for the fabrication of pixel detectors.

III. SOI ON HIGH-RESISTIVITY PROCESS

In the second phase of the project, a full "SOI-on-HΩ" process was executed at IMEC. The starting material was n-type <100> 1500 Ωcm 5 inch diameter wafers.
SOI wafers were prepared in two ways:
a) laser-recrystallized ZMR wafers. These have a top layer thickness of 400 nm and a buried oxide thickness of 1000 nm. Lines of seeding dots are located on a 200 μm pitch.
b) SIMOX implanted wafers. The top layer thickness is 200 nm, the oxide layer is 400 nm.

An "SOI-HR" mask set was designed for this complete SOI-on-HΩ run. It contains test structures for evaluation of the CMOS process, and an SOI technology test chip. The bulk quality is evaluated on several types of diodes, capacitors, gated diodes, and bulk transistors. Structures to test the interconnects between top and bulk are also available. Further the mask contains single amplifiers (adaptations of existing designs for the HR-diode read-out), and two larger "pixel-detectors" [8]. The complete test chip measures 1.3 x 3 cm.

The SOI-CMOS technology is derived from the IMEC 1 μm SOI process, but is used here with 3 μm line widths and layout rules.
The processing steps include:
- SOI layer preparation
- active area definition
- n-channel and p-channel conditioning (V_{th} adjust, film doping)
- gate poly definition
- bulk diode junction area definition
- n-type and p-type source-drain implant
- contact holes and single layer metallization
- passivation layer and bonding pad openings

The process was executed in the first half of 1992.

IV. "SOI-ON-HΩ": BULK BEHAVIOUR

For what concerns the devices in the substrate, the

relevance of this phase resides in the fact that the wafers have now undergone a full CMOS fabrication process, in addition to the special steps necessary for the substrate diodes.
Measurement results confirm the findings of the previous study. Profiles of the effective dopant concentration versus depth (obtained from C-V measurements on 1 cm^2 diodes) are shown in fig. 5. For the ZMR wafers the doping is uniform, about 2.5 x 10^{12} cm^{-3}, while in the SIMOX substrates the known peak concentration of 1 x 10^{13} cm^{-3} is seen at a depth of 40-50 μm. Due to the higher thickness of the wafers (625 μm) and the lower initial resistivity, the total depletion voltage is about 730 V for the uniformly doped ZMR wafers, and even higher for the SIMOX. Junction breakdown did prevent to profile down to the back surface, but a rising concentration beyond 500 μm is a hint of the presence of a second peak at the backside.

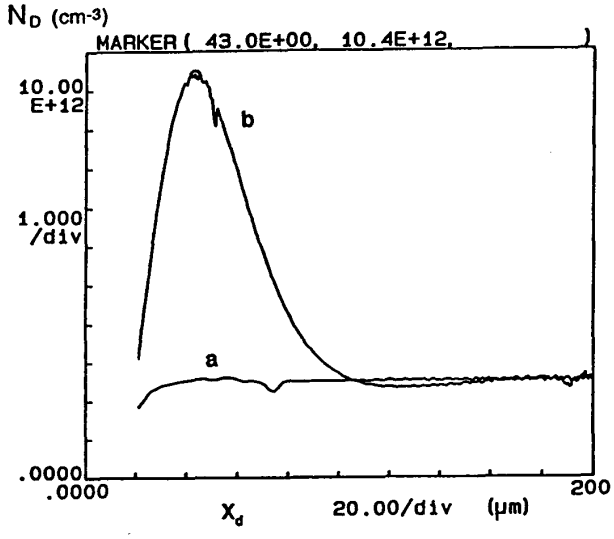

Fig.5 Profile of effective donor density versus depletion depth in the substrate: a) on laser-ZMR wafer, b)on SIMOX wafer. f = 100 KHz.

Further evidence for the plausibility of the interpretation of these peaks as due to oxygen-related "thermal donors", which are activated at around 450 °C, came from the following experiment: One wafer was withdrawn before the final metallization sintering, and profiled: the peak was still visible, but about one third as high as for the sintered wafers. Subsequently the wafers was sintered, and the peak grew to the level of the other wafers. The possibility exists to modify the thermal schedule of the process in order to reduce the amount of these donors (they are known to annihilate around 600 °C).

The leakage currents achieved in the first complete processing, which are significantly lower than the values found in the feasibility study, are typically 5 to 20 nA/cm^2 at 100 V bias; the difference between ZMR and SIMOX is now hardly significant. The corresponding values of the carrier generation lifetimes are 0.5 - 1 ms for the ZMR and 0.3 - 0.6 ms for the SIMOX.
Surface generation at the depleted (bulk silicon) - (buried SOI oxide) interface has been evaluated with gate-controlled diodes specifically designed for this purpose, featuring interdigitated gate and diode electrodes. The surface generation velocity is in the range 15 - 20 cm/s for both ZMR and SIMOX. The interface between the substrate and the SOI oxide was also studied by standard high frequency and quasistatic C-V measurements on MOS capacitors. The curves for a ZMR wafer are shown in Fig. 6. From these, a total effective oxide charge $N_{eff} \approx 7 \times 10^{10}$ cm^{-2} can be derived, and an interface trap density at midgap $D_{it} \approx 3 \times 10^{10}$ $cm^{-2}eV^{-1}$. These values are only an order of magnitude higher than the best thermal oxides grown on (100) substrates. For the SIMOX samples, the technique gave inconsistent results.

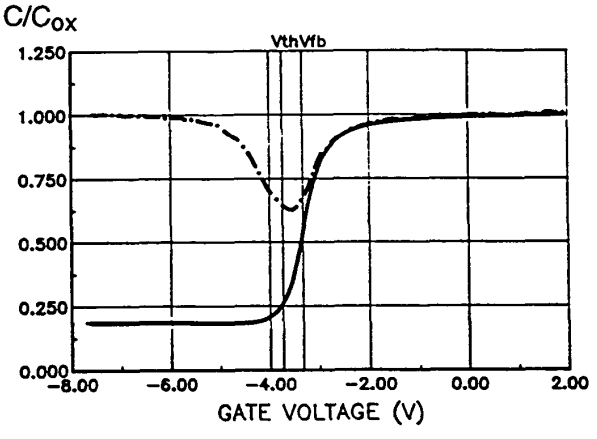

Fig.6 High frequency (100 kHz, solid line) and quasistatic (dotted line) C-V curves for a MOS capacitor on a laser-ZMR wafer.

V. "SOI-ON-HΩ": MOSFET BEHAVIOUR

We considered MOSFETs (Fig. 7a), lateral diodes, sheet resistances and metal interconnects as basic top layer devices. Of these the properties of the MOSFETs are especially important for the following reasons:
•the so-called "kink", a typical non-linearity in the I_D-V_{DS} characteristics of SOI MOSFETs, and the possible suppression of it.
•the coupling of the MOSFET current level to the potential in the substrate, or the back-gate effect. It is closely related with the first effect.
•low-frequency noise (1/f noise), as an important parameter for the envisaged applications.

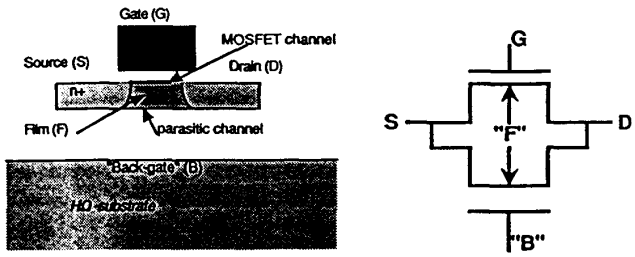

Fig.7 Schematic cross section of a nMOSFET in an SOI layer (a), and equivalent circuit (b). The normal MOS channel is driven by the gate (G) potential. Due to the SOI device nature, there exists a second parasitic channel at the backside of the film. The "back gate" (B), i.e. the surface potential in the high-resistivity substrate, influences both the backside and the front side channel. The film (F) plays the role of the "bulk" terminal in a "classical" MOSFET. An undepleted film is useful in avoiding the kink and reducing the backside - front side coupling.

Except for a high V_{th} in the pMOSFETs (-2.0 V), MOSFET operation is excellent. The kink can be suppressed by explicitly grounding the film, as illustrated in fig.8. The kink effect can be understood as an uncontrolled varying "film"-source voltage (V_{FS}), changing the drain current through the bulk effect (Fig.8 and 9).

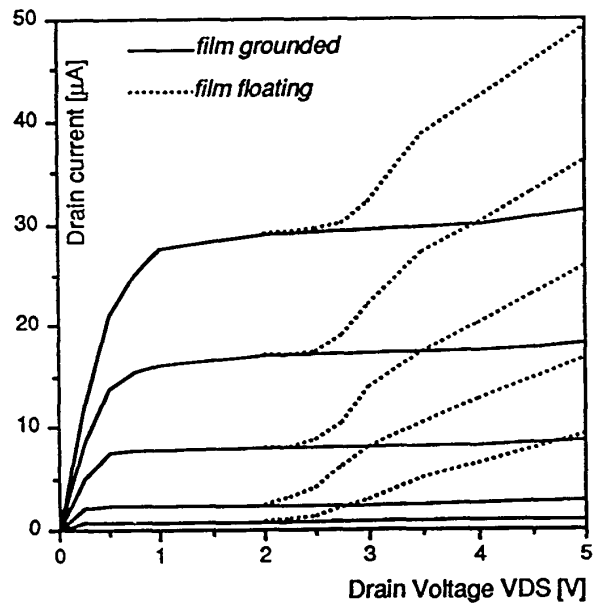

Fig.8 I_D/V_{DS} characteristics of an SOI nMOSFET; W=10 µm; L=10µm; V_{BS}=0; V_{GS} = 1, 1.25, 1.5, 1.75 and 2 V. Plain line: film contact grounded (V_{FS}=0). Dashed line: film contact floating (unconnected).

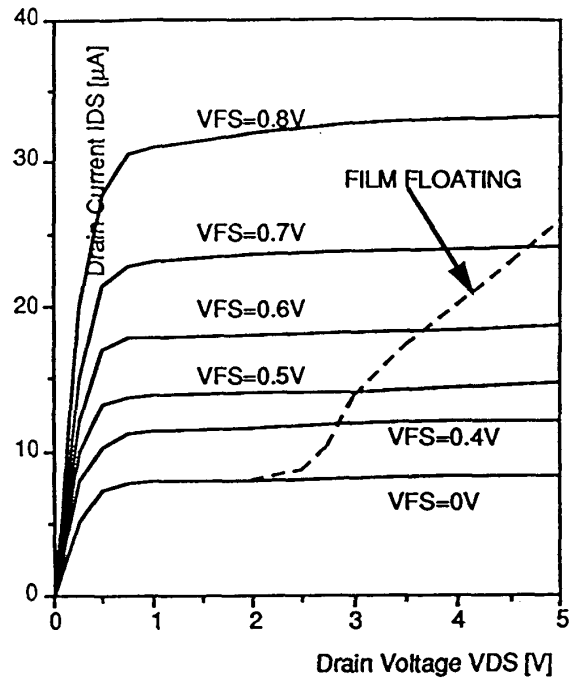

Fig.9 I_D/V_{DS} characteristics of an SOI nMOSFET, for a fixed V_{GS} = 1.5 V and V_{BS} = 0 V, and a set of film voltages V_{FS}. The dashed line is the curve for a floating film contact.

A second effect in SOI MOSFETs that is not seen in bulk MOSFETs is rising from the fact that an SOI MOSFET consists of actually two MOSFETs, placed back-to-back (Fig. 7b). The top transistor is the one intended by the circuit designer, yet there always is a parasitic "backside" MOSFET that shares the source, drain and film of the top MOSFET, but has the SOI substrate potential as gate. In the envisaged application, typically MOSFET circuitry on top of PIN detectors, fluctuations in the detector potential will possibly feed-back to the MOSFET's parasitic mode of conduction. Grounding the film reduces a bit the coupling of the substrate potential to the MOSFET current. Heavy counter-doping the parasitic backside channel will prevent backside conduction. This type of implantation is a critical step in the process, as it must cut off the backside channel without affecting the normal front side channel. This, and radiation hardness, are reasons to prefer a silicon film thickness of more than 200 nm.

Results on the low-frequency noise on MOSFETs obtained from this process are summarized in Table 1. They are slightly worse, but comparable with typical values for a bulk CMOS process used in analog design (LUVCMOS 3U0, IMEC). As a figure of merit we use the Kf factor, as defined by a widely used empirical relation for the equivalent gate

noise spectral density ($S_{V_{Geq}}$) in silicon MOSFETs:

$$S_{V_{Geq}}(f) = Kf/W.L.f \qquad (1)$$

where W and L are the transistor's width and length, and f is the frequency.

process	SOI-on-HΩ SIMOX	LUVCMOS
nMOSFETs	$Kf = 3.8 \times 10^{-20}$	2.0×10^{-20}
pMOSFETs	$Kf = 4.5 \times 10^{-20}$	3.0×10^{-21}

Table 1. Average Kf $[V^2m^2]$ obtained from low frequency noise measurements. 10 MOSFETs of different sizes were measured at several working points. Measurement frequency f is 1 Hz. Drain currents ranging from nA to mA. No significant dependence of the Kf values on the working point was seen.

VI. CONCLUSIONS

The results of the project have proven the feasibility of the monolithic integration of particle detectors and associated electronics. In the SOI top layer (CMOS) devices have a quality that is comparable to bulk CMOS technologies. Also the operation of large analog/digital circuits was demonstrated (i.e. arrays of detector/amplifiers). SIMOX is the material of choice for the top layer devices, as the reproducibility and yield is high, and it does not require the presence of a grid of seeding points and anti-reflective stripes as is used for the laser-ZMR process. A problem area for the design of top layer electronics is the kink non-linearity and the back-gate effect of the top layer MOSFETs. These will be optimized in the scheduled processing runs.

With reference to the detecting elements in the substrate, ZMR wafers give very good results. For SIMOX wafers, the main concern is the higher depletion voltage resulting from the increase in effective doping concentration. Optimization of the process may lead to a reduction of this effect. In addition, charge trapping and radiation damage effects need to be investigated.

For the first time a co-integration of CMOS electronics and high-resistivity PIN-detectors has been demonstrated using an SOI approach.

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